IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Michael P. Belyansky, *et al.*

Docket No. P27154

Confirmation No. 2429

Group Art Unit: 2818

Examiner: A. Huynh

Appln. No. : 10/708,430

Filed : March 3, 2004

For : **MOBILITY ENHANCED CMOS DEVICES**

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AMENDMENT UNDER 37 C.F.R. §1.114

Sir:

Please amend the above-identified application as follows.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefore (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. 09-0458.

Amendments to the claims begin on page 2; and

Remarks begin on page 9.

AMENDMENT TO THE CLAIMS

Please **ADD** new claims 38-47 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) A method of forming a semiconductor structure comprising steps of:

forming spacer voids between a gate of a mandrel layer;

creating recesses in a substrate below and in alignment with the spacer voids;

filling a first portion of the recesses with a stress imposing material;

filling a second portion of the recesses with a semiconductor material; and

removing the mandrel layer.

2. (Original) A method according to claim 1, further including forming dummy spacers between the mandrel layer and the gate and forming a nitride interface as an etch stop in the recesses.

3. (Original) A method according to claim 1, wherein the recesses include a first recess and a second recess, the first recess and the second recess having a depth greater than a depth of the bottom of a channel area of the gate.

4. (Previously Presented) A method according to claim 3, wherein the first recess has a depth substantially equal to a depth of the second recess.

5. (Original) A method according to claim 3, wherein the first recess has a depth of about 500 to 2000 angstroms.

6. (Original) A method according to claim 1, further comprising forming dummy spacers and removing the dummy spacers to form the spacer voids, wherein:

a first dummy spacer has a first width;

a second dummy spacer has a second width;

a first recess of the recesses has a width substantially equal to the first width of the first dummy spacer; and

a second recess of the recesses has a width substantially equal to the second width of the second dummy spacer.

7. (Original) A method according to claim 6, wherein the first width is substantially equal to the second width.

8. (Original) A method according to claim 7, wherein the first width is about 100 to 1000 Å.

9. (Original) A method according to claim 1, wherein the recesses are substantially equidistant from the gate.

10. (Original) A method according to claim 1, wherein the stress imposing material is a material that introduces a compressive stress.

11. (Original) A method according to claim 1, wherein the stress imposing material is a material that introduces a tensile stress.

12. (Original) A method according to claim 1, wherein the stress imposing material is a material that introduces a stress that degrades electron or hole mobility in the semiconductor structure.

13. (Original) A method according to claim 1, wherein the stress imposing material is a material that introduces a stress that enhances electron or hole mobility in the semiconductor structure.

14. (Original) A method according to claim 1, wherein the stress imposing material is a material comprised of at least one of polysilicon, SiO_2, $Si_{1-x}Ge_x$, Si_xN_y, or Si_xON_y.

15. (Original) A method according to claim 1, wherein the semiconductor material is comprised of epitaxially grown Si.

16. (Original) A method according to claim 1, wherein: the gate is an n-channel field effect transistor gate; and the stress imposing material is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate.

17. (Original) A method according to claim 1, wherein: the gate is a p-channel field effect transistor gate; and the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

18. (Previously Presented) A method according to claim 1, further comprising a step of annealing after filling the first portion of the recesses with the stress imposing material.

19. (Previously Presented) A method of forming a semiconductor structure comprising steps of:

forming dummy spacers on sides of a gate formed on a substrate;

forming a mandrel layer with portions of the mandrel layer abutting the dummy spacers;

removing the dummy spacers to form spacer voids between the gate and the mandrel layer;

creating recesses in the substrate below and in alignment with the spacer voids;

filling a first portion of the recesses with a stress imposing material; and

filling a second portion of the recesses with a semiconductor material.

20. (Previously Presented) A method according to claim 19, further comprising the step of:

removing the mandrel layer,

wherein:

the first portion of the recesses is below the bottom of a channel area of the gate; and

the stress imposing material is a material that introduces one of a compressive stress and a tensile stress in the channel area.

21. (Original) A method according to claim 19, wherein the stress imposing material is a material comprised of at least one of polysilicon, SiO_2, $Si_{1-x}Ge_x$, Si_xN_y, or Si_xON_y.

22. (Original) A method according to claim 20, wherein the gate is one of:

an n-channel field effect transistor gate and the stress imposing material is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate; and

a p-channel field effect transistor gate and the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

Claim 23 (Canceled).

24. (Previously Presented) A method according to claim ~~23~~ 31, wherein the steps are performed in the order recited.

25. (Previously Presented) A method according to claim ~~23~~ 31, wherein one of:

the field effect transistor gate is an n-channel field effect transistor gate and the stress imposing material configured to enhance performance of the n-channel field effect transistor gate is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate; and

the field effect transistor gate is a p-channel field effect transistor gate and the stress imposing material configured to enhance performance of the p-channel field effect transistor gate is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate.

Claims 26-30 (Canceled).

31. (Previously Presented) A method of forming a semiconductor structure comprising steps of:

forming a field effect transistor gate on a substrate;

forming a first dummy spacer and a second dummy spacer on sides of the field effect transistor gate;

forming a mandrel layer with portions of the mandrel layer abutting the first and second dummy spacers for the field effect transistor gate;

after masking the semiconductor structure, introducing stress to the field effect transistor gate; and

removing the mandrel layer,

wherein the step of introducing stress material comprises:

removing the first and second dummy spacers from the field effect transistor gate to form first and second spacer voids between the field effect transistor gate and the portions of the mandrel layer;

creating a first recess in the substrate below and in alignment with the first spacer void and a second recess in the substrate below and in alignment with the second spacer void for the field effect transistor gate;

filling a first portion of the first recess and a first portion of the second recess with a stress imposing material configured to enhance performance of the field effect transistor gate;

filling a second portion of the first recess and a second portion of the second recess for the field effect transistor gate with a semiconductor material; and

unmasking the semiconductor structure.

32. (Previously Presented) A method according to claim 31, wherein the stress imposing material is a material that introduces a compressive stress.

33. (Previously Presented) A method according to claim 31, wherein the stress imposing material is a material that introduces a tensile stress.

34. (Previously Presented) A method according to claim 31, wherein the stress imposing material is a material that introduces a stress that degrades electron or hole mobility in the semiconductor structure.

35. (Previously Presented) A method according to claim 31, wherein the stress imposing material is a material that introduces a stress that enhances electron or hole mobility in the semiconductor structure.

36. (Previously Presented) A method according to claim 31, wherein the stress imposing material is a material comprised of at least one of polysilicon, SiO_2, $Si_{1-x}Ge_x$, Si_xN_y, or Si_xON_y.

37. (Previously Presented) A method according to claim 31, wherein the semiconductor material is comprised of epitaxially grown Si.

38. (new) A method of providing compressive or tensile imposing materials selectively beneath and in alignment with spacer areas of a semiconductor substrate

and adjacent to channel areas to enhance electron and hole mobility in CMOS circuits, comprising:

forming disposable dummy spacers on the semiconductor substrate and adjacent to the channel areas of a patterned gate;

forming a mandrel over active device regions of the patterned gate, abutting the disposable dummy spacers.

after forming of the mandrel, removing the disposable dummy spacers to form spacer voids;

etching recesses into the semiconductor substrate at a bottom of the spacer voids;

introducing a compressive or tensile imposing material into a portion of the recesses; and

filling a remainder of the recesses with material.

39. (new) The method of claim 38, wherein the compressive or tensile imposing material fill the recesses up to about a surface of the semiconductor substrate.

40. (new) The method of claim 39, wherein:

the compressive imposing material undergoes a volume expansion to impart compressive stresses; and

the tensile imposing material undergoes a volume contraction to impart tensile stresses.

41. (new) The method of claim 38, wherein a depth of the recesses are approximately 500 to 2000 Angstroms.

42. (new) The method of claim 38, wherein the recesses are partially filled with the compressive or tensile imposing material.

43. (new) The method of claim 38, wherein the disposable dummy spacers are comprised of a nitride.

44. (new) The method of claim 38, wherein the disposable dummy spacers are comprised of a SiO_2 liner and a polysilicon film.

45. (new) The method of claim 38, wherein the mandrel is comprised of a dielectric film or a self-planarizing material that withstands etching of the disposable dummy spacers.

46. (new) The method of claim 38, further comprising forming a nitride interface in the recesses.

47. (new) The method of claim 38, wherein:

the tensile imposing material is a dielectric film or polysilicon which is annealed by rapid thermal annealing (RTA) between 950 to 1050°C such that polysilicon grains grow and experience a volume contraction to create a tensile stress; and

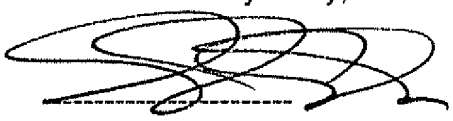
the compressive imposing material is a dielectric film, $Si_{1-x}Ge_x$ or SiO_2.

REMARKS

Claims 1-22, 24, 25 and 31-47 are currently pending in the application. Claims 38-47 have been added for consideration by the Examiner. Support for the new claims can be found in at least figures 1-7 and the description thereof. No new matter has been added. Applicants are filing this amendment with a Request for Continued Examiner and a Petition to Withdraw the Payment of the Issue Fee.

Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458.

Respectfully submitted,
Michael P. Belyansky, *et al.*



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